CLAIMS

What is claimed is:

1. A method comprising:
accessing a label stack of a received packet, the label stack including a plurality of multiprotocol label switching (MPLS) labels;
reading from an incoming label mapping (ILM) table stored in a first memory an entry associated with a top MPLS label in the label stack and a number of other entries;
storing the number of other entries read from the ILM table in a second memory.

2. The method of claim 1, further comprising performing an action associated with the top MPLS label.

3. The method of claim 2, further comprising:
accessing one of the number of other ILM entries stored in the second memory, the one ILM entry associated with a next MPLS label in the label stack; and
performing an action associated with the next MPLS label.

4. The method of claim 1, further comprising:
reading from the ILM table stored in the first memory a number of additional entries; and
storing in the second memory the additional number of ILM entries read from the first memory.

5. The method of claim 1, wherein the plurality of MPLS labels of the label stack are in sequence.

6. The method of claim 1, wherein the plurality of MPLS labels of the label stack are out of sequence.

7. The method of claim 6, wherein the ILM table comprises a hash table.

8. The method of claim 1, wherein the first memory comprises an external memory and the second memory comprises an on-chip memory.

9. The method of claim 1, wherein the first memory comprises part of an on-chip memory subsystem coupled with a processing engine, and wherein the second memory comprises an on-chip memory associated with the processing engine.

10. A device comprising:
a processing system; and
an on-chip memory coupled with the processing system;
wherein the processing system is programmed to perform operations including
accessing a label stack of a received packet, the label stack including a plurality of multiprotocol label switching (MPLS) labels;
reading from an incoming label mapping (ILM) table stored in a second memory an entry associated with a top MPLS label in the label stack and a number of other entries;
storing the number of other entries read from the ILM table in the on-chip memory.

11. The device of claim 10, wherein the processing system is programmed to perform operations further comprising performing an action associated with the top MPLS label.

12. The device of claim 11, wherein the processing system is programmed to perform operations further comprising:
accessing one of the number of other ILM entries stored in the on-chip memory, the one ILM entry associated with a next MPLS label in the label stack; and
performing an action associated with the next MPLS label.

13. The device of claim 10, wherein the processing system is programmed to perform operations further comprising:
reading from the ILM table stored in the second memory a number of additional entries; and
storing in the on-chip memory the additional number of ILM entries read from the second memory.

14. The device of claim 10, wherein the plurality of MPLS labels of the label stack are in sequence.

15. The device of claim 10, wherein the plurality of MPLS labels of the label stack are out of sequence.

16. The device of claim 15, wherein the ILM table comprises a hash table.

17. The device of claim 10, wherein the second memory comprises another on-chip memory coupled with the processing system.

18. The device of claim 10, wherein the second memory comprises an external memory.

19. The device of claim 10, wherein the processing system comprises one of a number of processing engines.

20. The device of claim 19, wherein the on-chip memory comprises part of the one processing engine.

21. The device of claim 19, wherein the on-chip memory comprises a memory subsystem coupled with the number of processing engines.

22. An apparatus comprising:

a memory; and

a processing device coupled with the memory, the processing device including a processing system and an on-chip memory coupled the processing system;

wherein the processing system is programmed to perform operations including

accessing a label stack of a received packet, the label stack including a plurality of multiprotocol label switching (MPLS) labels;

reading from an incoming label mapping (ILM) table stored in the memory an entry associated with a top MPLS label in the label stack and a number of other entries;

storing the number of other entries read from the ILM table in the on-chip memory.

23. The apparatus of claim 22, wherein the processing system is programmed to perform operations further comprising performing an action associated with the top MPLS label.

24. The apparatus of claim 23, wherein the processing system is programmed to perform operations further comprising:

accessing one of the number of other ILM entries stored in the on-chip memory, the one ILM entry associated with a next MPLS label in the label stack; and

performing an action associated with the next MPLS label.

25. The apparatus of claim 22, wherein the processing system is programmed to perform operations further comprising:

reading from the ILM table stored in the memory a number of additional entries; and

storing in the on-chip memory the additional number of ILM entries read from the memory.

26. The apparatus of claim 22, wherein the plurality of MPLS labels of the label stack are in sequence.

27. The apparatus of claim 22, wherein the plurality of MPLS labels of the label stack are out of sequence.

28. The apparatus of claim 27, wherein the ILM table comprises a hash table.

29. The apparatus of claim 22, wherein the processing system comprises one of a number of processing engines.

30. The apparatus of claim 29, wherein the on-chip memory comprises part of the one processing engine.

31. The apparatus of claim 29, wherein the on-chip memory comprises a memory subsystem coupled with the number of processing engines.

32. An article of manufacture comprising:
a machine accessible medium providing content that, when accessed by a machine, causes the machine to
access a label stack of a received packet, the label stack including a plurality of multiprotocol label switching (MPLS) labels;
read from an incoming label mapping (ILM) table stored in a first memory an entry associated with a top MPLS label in the label stack and a number of other entries;
store the number of other entries read from the ILM table in a second memory.

33. The article of manufacture of claim 32, wherein the content, when accessed, further causes the machine to perform an action associated with the top MPLS label.

34. The article of manufacture of claim 33, wherein the content, when accessed, further causes the machine to:
access one of the number of other ILM entries stored in the second memory, the one ILM entry associated with a next MPLS label in the label stack; and
perform an action associated with the next MPLS label.

35. The article of manufacture of claim 32, wherein the content, when accessed, further causes the machine to:
read from the ILM table stored in the first memory a number of additional entries; and
store in the second memory the additional number of ILM entries read from the first memory.

36. The article of manufacture of claim 32, wherein the plurality of MPLS labels of the label stack are in sequence.

37. The article of manufacture of claim 32, wherein the plurality of MPLS labels of the label stack are out of sequence.

38. The article of manufacture of claim 37, wherein the ILM table comprises a hash table.

39. The article of manufacture of claim 32, wherein the first memory comprises an external memory and the second memory comprises an on-chip memory.

40. The article of manufacture of claim 32, wherein the first memory comprises part of an on-chip memory subsystem coupled with a processing engine, and wherein the second memory comprises an on-chip memory associated with the processing engine.

41. A system comprising:
a system memory coupled with a bus;
a program memory coupled with the bus, the program memory to store a set of instructions; and
a processing device coupled with the bus, the processing device including a processing system and an on-chip memory coupled the processing system;
wherein the processing system, when executing the set of instructions, performs operations including
accessing a label stack of a received packet, the label stack including a plurality of multiprotocol label switching (MPLS) labels;
reading from an incoming label mapping (ILM) table stored in the system memory an entry associated with a top MPLS label in the label stack and a number of other entries;
storing the number of other entries read from the ILM table in the on-chip memory.

42. The system of claim 41, wherein the processing system, when executing the set of instructions, performs operations further comprising performing an action associated with the top MPLS label.

43. The system of claim 42, wherein the processing system, when executing the set of instructions, performs operations further comprising:
accessing one of the number of other ILM entries stored in the on-chip memory, the one ILM entry associated with a next MPLS label in the label stack; and
performing an action associated with the next MPLS label.

44. The system of claim 41, wherein the processing system, when executing the set of instructions, performs operations further comprising:
reading from the ILM table stored in the system memory a number of additional entries; and
storing in the on-chip memory the additional number of ILM entries read from the memory.

45. The system of claim 41, wherein the plurality of MPLS labels of the label stack are in sequence.

46. The system of claim 41, wherein the plurality of MPLS labels of the label stack are out of sequence.

47. The system of claim 46, wherein the ILM table comprises a hash table.

48. The system of claim 41, wherein the program memory comprises a read only memory (ROM).

49. A method comprising allocating a number of multiprotocol label switching (MPLS) labels for a local forwarding equivalence class (FEC) at an edge node of an MPLS domain in sequence.

50. The method of claim 49, wherein the edge node supports a number of local FECs, the method further comprising maintaining a separate label space for each local FEC.

51. The method of claim 49, further comprising allocating at least some of the MPLS labels associated with the local FEC in ascending order from an outermost tunnel to an innermost tunnel.